RoHS Compliant 8.5Gb/s Short Wavelength SFP+ Transceiver

FEATURES

- **Compliant with SFP+ MSA, SFF-8431 specification and Fiber Channel FC-PI-4**
- **Compliant with SFF-8472 MSA**
- **850nm VCSEL laser**
- **Built-in digital diagnostic monitoring function**
- **Backward compatible to 2G/4G Fiber Channel**
- **Duplex LC connector**
- **Power consumption ＜1W**
- **Laser Class 1 Product which comply with the requirements of IEC 60825-1 and IEC 60825-2**

Description

The LCP-8500A4EDR is hot pluggable 3.3V Small-Form-Factor transceiver modules designed expressly for high-speed communication applications that require rates of up to 8.5Gb/s.

It is compliant with SFP+ MSA, SFF-8431 specification and Fiber Channel FC-PI-4, as well as MSA SFF-8472.

The LCP-8500A4EDR transceivers provide with the LC receptacle that is compatible with the industry standard LC™ connector. The transceiver is also compatible with industry standard RFT connector and cage.

The post-amplifier of the LCP-8500A4EDR also includes a LOS (Loss Of Signal) circuit that provides a TTL logic-high output when an unusable optical signal level is detected.

The LCP-8500A4EDR transceiver is a Class 1 eye safety product. The optical power levels, under normal operation, are at eye safe level.

Applications

- High-speed storage area networks
- Computer cluster cross-connect
- Custom high-speed data pipes

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	T_S	-40		85	ºC	
Supply Voltage	V_{CC}	0		4	V	
Relative Humidity	RH	5		95	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	T_C	-5		70	ºC	
Supply Voltage	V_{CC}	3.135		3.465	V	
Data Rate			8.5	9	Gbps	

Electrical Characteristics

(V_{CC}=3.135V to 3.465V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Total Supply Current	I_{CC}		180	300	MA	
Transmitter						
Differential Input Voltage	Vin,pp	120		1000	mVppd	1
Data Input Rise/Fall Time		15		40	Ps	2
Transmitter Disable Input-High	V_{DISH}	2		V_{CC}+0.3	V	
Transmitter Disable Input-Low	V_{DISL}	0		0.8	V	
Transmitter Fault Output-High	V_{TXFH}	2		V_{CC}+0.3	V	
Transmitter Fault Output-Low	V_{TXFL}	0		0.8	V	
Receiver						
Differential Output Voltage	$V_{out,pp}$	300		1000	mVppd	3
Data Output Rise/Fall Time				45	Ps	1
LOS Output Voltage-Low	V_{LOSH}	2		V_{CC}+0.3	V	
LOS Output Voltage-High	V_{LOSL}	0		0.8	V	
RS0, RS1	V_{IL}	-0.3		0.8	V	4
	V_{IH}	2.0		Vcc+0.3	V	

Notes:

1. Internally AC coupled and terminated to 100 Ohm differential load.
2. These are 20%~80% values.
3. Internally AC coupled, but requires a 100 Ohm differential termination at or internal to Serializer/ Deserializer.
4. Shall be pulled low to VeeT with a ＞30k ohms resistor in the module.

Optical Characteristics

(V_{CC}=3.135V to 3.465V, Data Rate=8.5Gb/sec, PRBS=2^7-1 NRZ, 50/125μm MMF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Output Optical Power (Avg.)	P_O	-8.2		-1.8	dBm	
Optical Modulation Amplitude	OMA	302			μW	1
Center Wavelength	λ	840	850	860	nm	
Spectral Width (RMS)	σ			0.65	nm	
Optical Rise/Fall Time (20% - 80%)	t_r/ t_f			50/50	ps	2
RIN12OMA				-128	dB/Hz	3
Output Eye	Complies with the ANSI FC-PI-4 Rev. 6.01 specification, and is class 1 laser eye safety					
Receiver						
Sensitivity in OMA @8.5Gbps @4.25Gbps @2.125Gbps	P_{IN}			76 61 49	μW	4
Input Optical Wavelength	λ	840	850	860	nm	
Average Received Power, max	Rmax	0			dBm	
LOS-De-asserted (Avg.)	P_D			-14	dBm	
LOS-Asserted (Avg.)	P_A	-30			dBm	
LOS-Hysteresis	P_D -P_A	0.5			dB	
Optical Return Loss	ORL	12			dB	

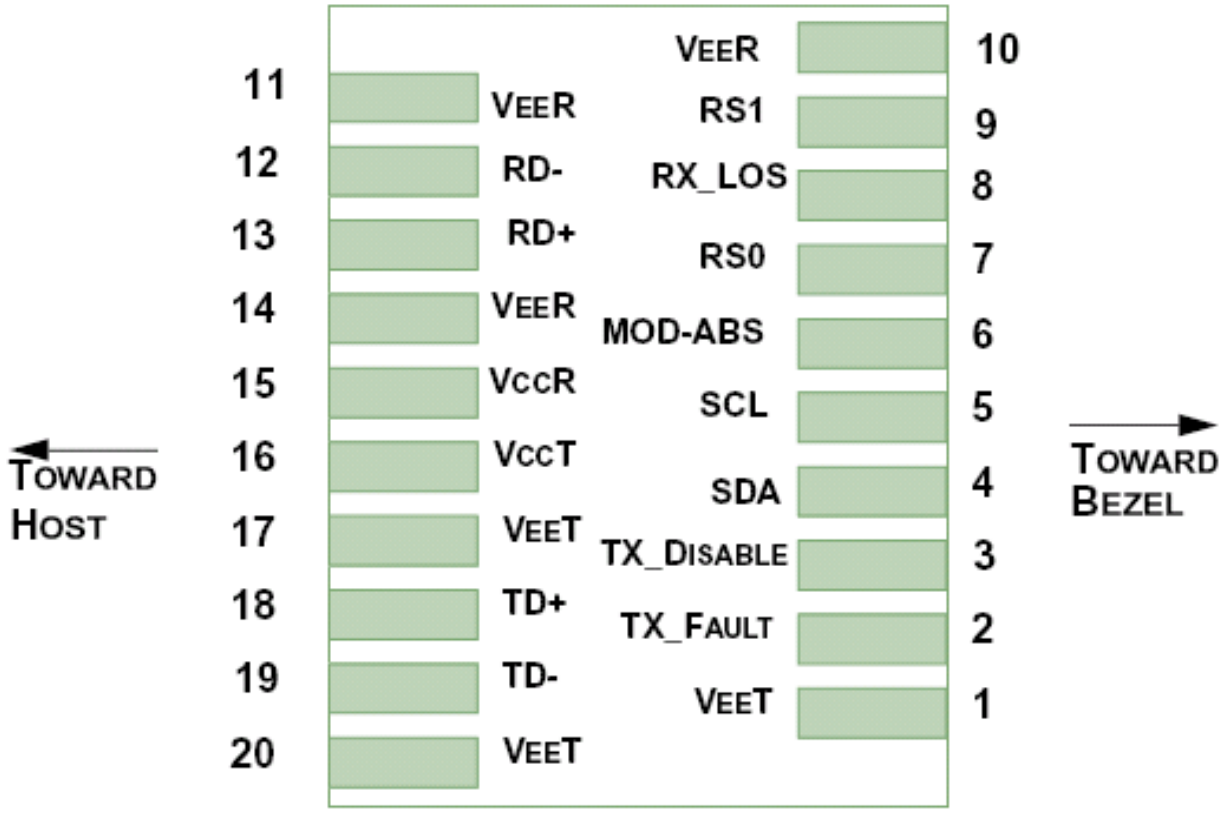
Link Length

Data Rate/Standard	Fiber Type	Modal Bandwidth @850nm (MHz*km)	Distance Range(m)	Notes.
8.5Gbps	62.5/125 μm MMF	200	0.5 to 21	5
	50/125 μm MMF	500	0.5 to 50	5
	50/125 μm MMF	900	0.5 to 90	5
	50/125 μm MMF	1500	0.5 to 120	5
	50/125 μm MMF	2000	0.5 to 150	5

Notes:

1. Equivalent extinction ratio specification for Fiber Channel. Allows smaller ER at higher average power.
2. Measured at nominal data rate. These are unfiltered 20%~80% values.
3. Transmitter Dispersion Penalty is measured using the methods specified in the IEEE standard 802.3-2005 Clause 52 except that the transversal filter differential delay is 33 ps.
4. The sensitivity is tested at a BER of 1×10^{-12} or better with an input signal consisting of 2^7-1 NRZ PRBS.
5. Distance, shown in the “Link Length” table, are calculated for worst case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques utilized in IEEE 802.3. In the nominal case, longer distances are achievable.

SFP+ Transceiver Electrical Pad Layout



Module Electrical Pin Definition

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	Transmitter Disable; Turns off transmitter laser output	3
4	LVTTL-I/O	SDA	2- write Serial Interface Data Line	
5	LVTTL-I/O	SCL	2- write Serial Interface Clock	
6		MOD_ABS	Module Absent, connected to V_{ee}T or V_{ee}R in the module	4
7	LVTTL-I	RS0	Rate Select 0, optionally controls SFP+ module receiver. When High input data rate>4.25GBd and when LOW input data rate ≦ 4.25GBd.	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication	2
9	LVTTL-I	RS1	Not Implement	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverter Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3V Supply	
16		VccT	Module Transmitter 3.3V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10k ohms to Host_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10k ohms to VccT in the Module.
4. This pin shall be pulled up with 4.7k-10k ohms to Host_Vcc on the host board.

Low speed electrical control pins and 2-wire interface

In addition to the 2-wire serial interface, the SFP+ module has the following low speed pins for control and status:

- TX_Fault
- TX_Disable
- RS0/RS1
- MOD_ABS
- RX_LOS

1. TX_Fault

.TX_Fault is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety.

The TX_Fault output pin is an open drain/collector and must be pulled p to the Host_Vcc with 4.7k-10k ohms on the host board.

2. TX_Disable

TX_Disable is a module input pin. When TX_Disable is asserted High or Left open, the SFP+ module transmitter output must be turned off. The TX_DIS pin must be pulled up to VccT in the SFP+ module.

3. RS0/RS1

RS0 and RS1 are module input rate select pins and are pulled low to VeeT with a > 30kΩ resistor in the module. RS0 is an input hardware pin which optionally selects the optical receives data path rate coverage for an SFP+ module. RS1 is an input hardware pin which optionally selects the optical transmits path data rate coverage for an SFP+ module.

RS1 is commonly connected to VeeT or VeeR in the legacy SFP modules. The host needs to ensure that it will not be damaged if this pin is connected to VeeT or VeeR in the module.

4. MOD_ABS

Mod_ABS is pulled up to Host_Vcc with 4.7k-10k ohms on the host board and connected to VeeT or VeeR in the SFP+ module. MOD_ABS is then asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD_DEF0.

5. SCL/SDA

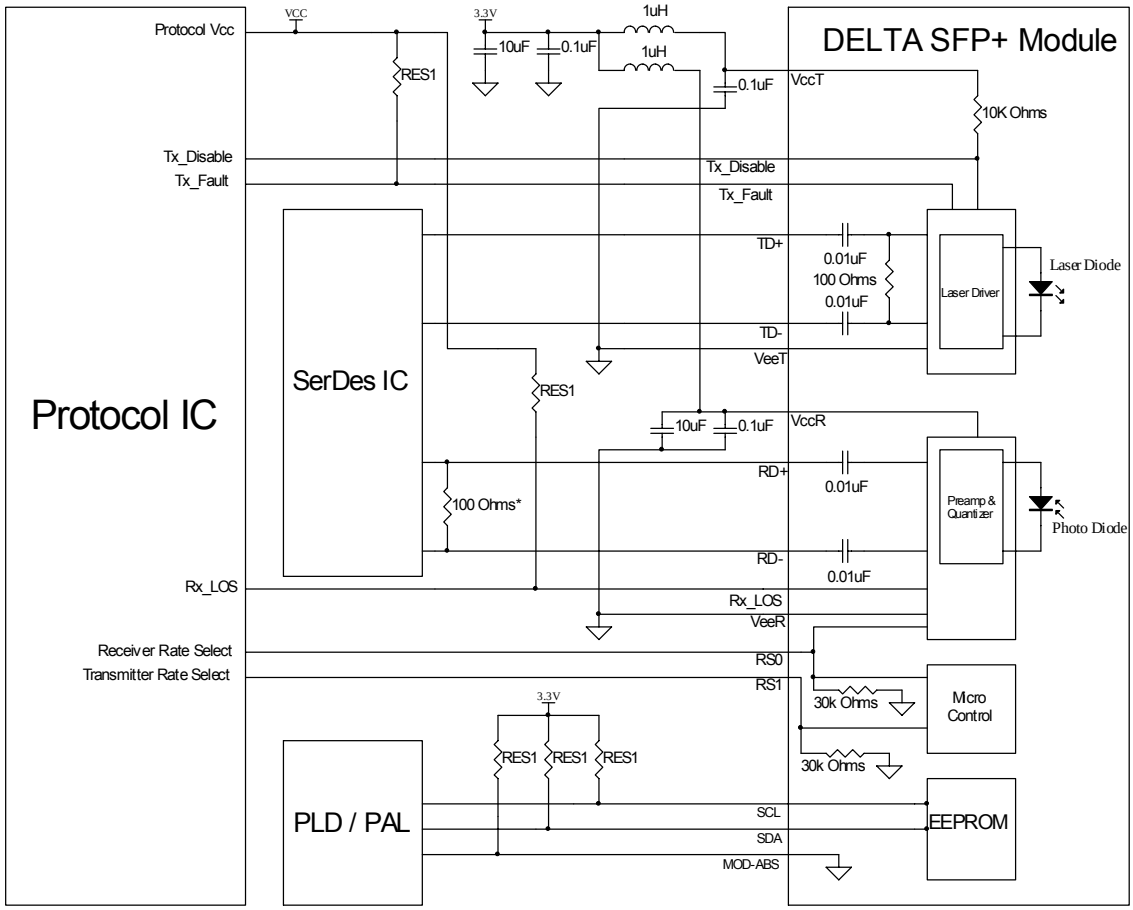
SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to a voltage in the range of 3.14V to 3.46V on the host.

6. RX_LOS

RX_LOS when High Indicated an optical signal level below that specified in the relevant standard. The RX_LOS pin is an open drain/collector outpit and must be pulled up to host Vcc with a 4.7k-10k ohms on the host board.

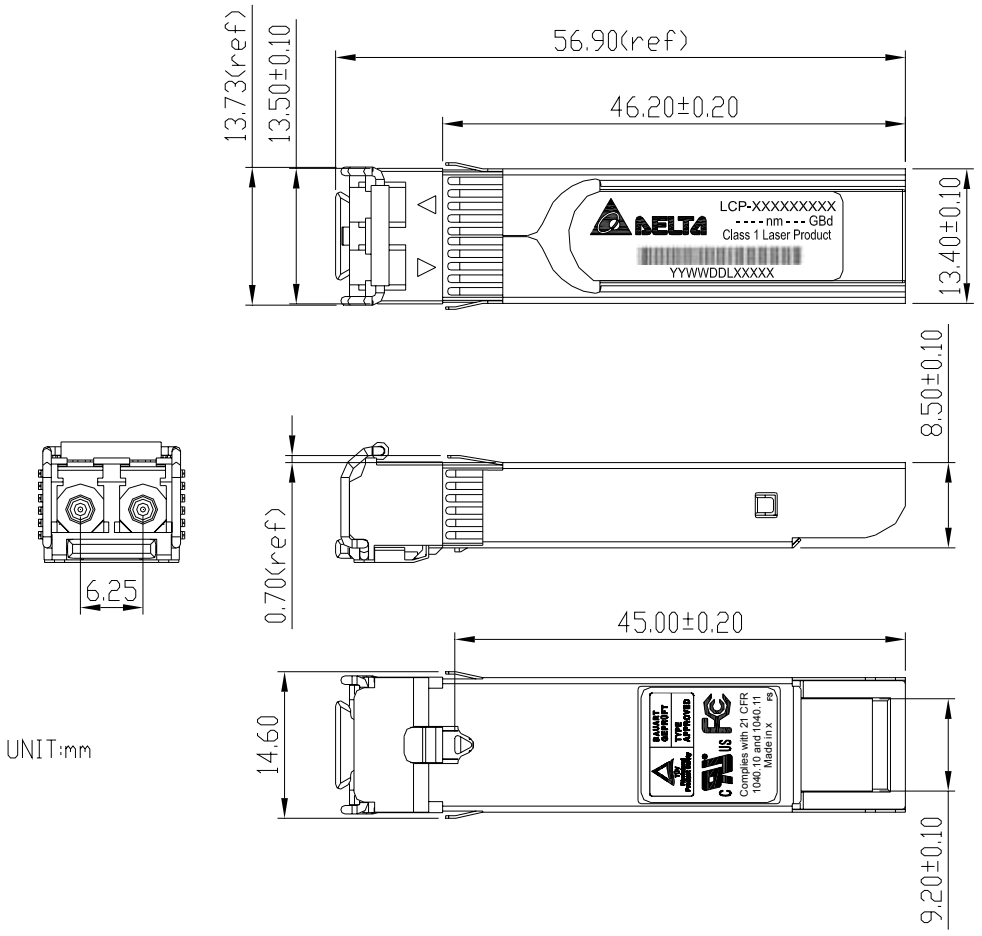
RX_LOS assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of RX_LOS a minimum hysteresis of 0.5 dBo is recommended.

Recommend Circuit Schematic



RES1 = 4.7k TO 10k Ohms
* Depands on SerDes IC used

Package Outline Drawing for Metal Housing with Bail de-latch



Timing parameters for SFP+ management

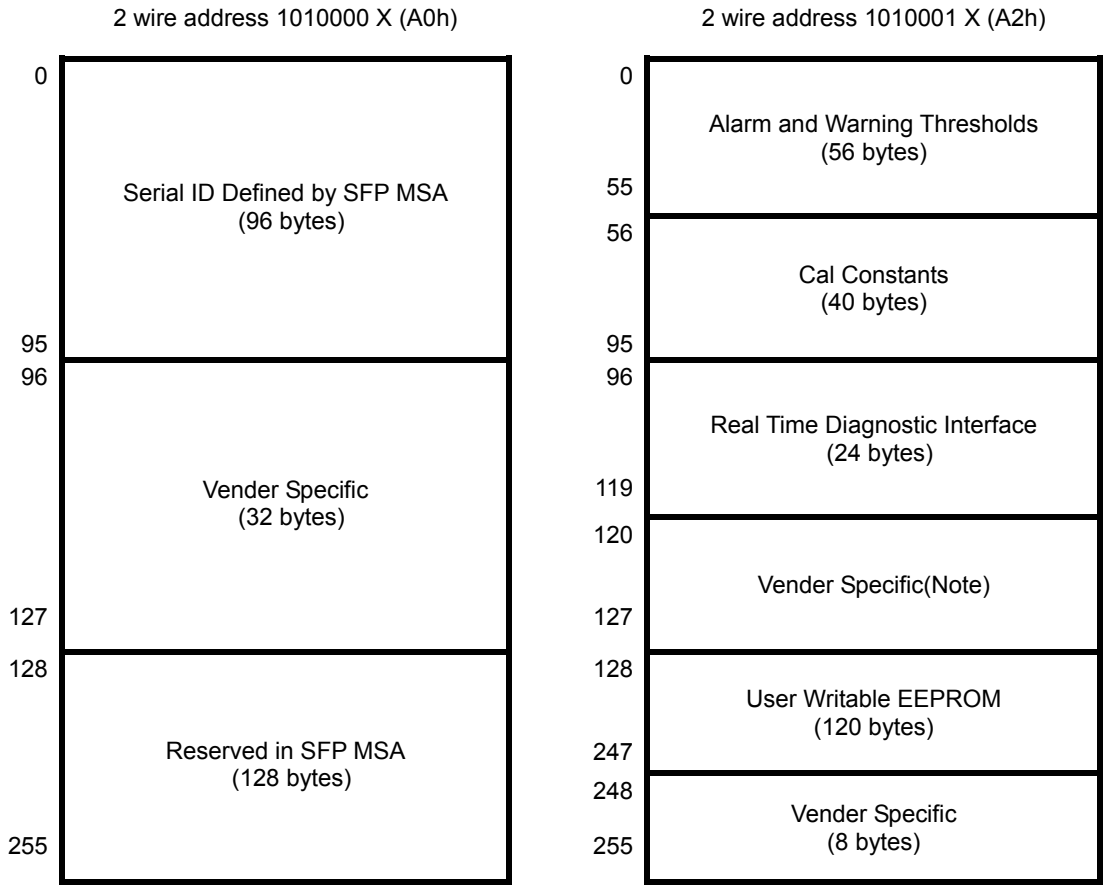
Parameter	Symbol	Min.	Max.	Unit	Note
TX_DISABLE Assert time	t_off		10	μsec	1
TX_DISABLE Negate time	t_on		2	msec	2
Time to initialize 2-wire interfase	t_2w_start_up		300	msec	3
Time to initialize	t_start_up		300	msec	4
Time to initialize cooled module	t_start_up_cooled		90	sec	4
Time to Power Up to Level 2	t_power_level2		300	msec	5
Time to Power Down from Level 2	T_power_down		300	msec	6
TX_Fault assert	TX_Fault_on		1	msec	7
TX_Fault assert for cooled module	TX_Fault_on		50	msec	7
TX_Fault Reset	t_reset	10		μsec	8
Module Reset	t_module_reset		TBD	msec	TBD
RS0, RS1 rate select timing for FC	t_RS0_FC, RS1_FC		500	μsec	9
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	msec	9
RX_LOS assert delay	t_los_on		100	μsec	10
RX_LOS negate delay	t_los_off		100	μsec	11

Notes:

1) Rising edge of TX_Disable to fall of output signal below 10% of nominal.
2) Falling edge of TX_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
3) From power on or negation of TX_Disable.
4) From power on or TX_Disable negated during power up, or TX_Fault recovery, until non-cooled power level 1 part (or non-cooled power level 2 part already enabled at power level 2 for TX_Fault recovery) is fully operational.
5) From falling edge of stop bit enabling power level 2 until non-cooled module is fully operational.
6) From falling edge of stop bit disabling power level 2 until module is within power level 1 requirements.
7) From Occurrence of fault to assertion of TX_Fault.
8) Time TX_Disable must be held High to reset TX_Fault.
9) From assertion till stable output.
10) From Occurrence of loss of signal to assertion of LOS.
11) From Occurrence of presence of signal to negation of RX_LOS.

Enhanced Digital Diagnostic Interface

The memory map in the following describes an extension to the memory map defined in SFP+ MSA. The enhanced interface uses the two wire serial bus address 1010001x (A2h) to provide diagnostic information about the module's present operating conditions.



Digital Diagnostic Memory Map Specific Data Field Descriptions

Note:

1) Write the password (11h, 11h, 11h, 11h) on the bytes of 123-126 of address A2h then the address of bytes 128-255 (User Writable) can be read and written.

EEPROM Serial ID Memory Contents (2-Wire Address A0h)

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
00	03		43	2D	-	86	DC	
01	04		44	38	8	87	DC	
02	07		45	35	5	88	DC	
03	03		46	30	0	89	DC	
04	00		47	30	0	90	DC	
05	00		48	41	A	91	DC	
06	00		49	34	4	92	68	
07	40		50	45	E	93	FA	
08	40		51	44	D	94	03	
09	0C		52	52	R	95	CS2	Note 4
10	54		53	30		96	00	
11	03		54	30		97	00	
12	55		55	30		98	00	
13	03		56	41		99	00	
14	00		57	20		100	00	
15	00		58	20		101	00	
16	05		59	20		102	00	
17	02		60	03		103	00	
18	00		61	52		104	00	
19	00		62	00		105	00	
20	44	D	63	CS1	Note 1	106	00	
21	45	E	64	00		107	00	
22	4C	L	65	3A		108	00	
23	54	T	66	00		109	00	
24	41	A	67	00		110	00	
25	20		68	SN	Note 2	111	00	
26	20		69	SN		112	00	
27	20		70	SN		113	00	
28	20		71	SN		114	00	
29	20		72	SN		115	00	
30	20		73	SN		116	00	
31	20		74	SN		117	00	
32	20		75	SN		118	00	
33	20		76	SN		119	00	
34	20		77	SN		120	00	
35	20		78	SN		121	00	
36	00		79	SN		122	00	
37	00		80	SN		123	00	
38	00		81	SN		124	00	
39	00		82	SN		125	00	
40	4C	L	83	SN		126	00	
41	43	C	84	DC	Note 3	127	00	
42	50	P	85	DC		128	00	Note5

Notes:

1) Byte 63: Check sum of bytes 0-62.
2) Byte 68-83: Serial number.
3) Byte 84-91: Date code.
4) Byte 95: Check sum of bytes 64-94.
5) Byte 128 to 255 had been set hex 00.

Digital Diagnostic Monitoring Interface

Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Value (Dec.)	Unit	Note
00-01	2	Temp High Alarm	T_C (MAX.)+15	℃	1
02-03	2	Temp Low Alarm	T_C (MIN.)		
04-05	2	Temp High Warning	T_C (MAX.)+10		
06-07	2	Temp Low Warning	T_C (MIN.)+10		
08-09	2	Voltage High Alarm	Vcc+5%	Volt	
10-11	2	Voltage Low Alarm	Vcc-5%		
12-13	2	Voltage High Warning	Vcc+3%		
14-15	2	Voltage Low Warning	Vcc-3%		
16-17	2	Bias High Alarm	I_{OP}+10	mA	2
18-19	2	Bias Low Alarm	I_{OP}-5		
20-21	2	Bias High Warning	I_{OP}+7		
22-23	2	Bias Low Warning	I_{OP}-3		
24-25	2	TX Power High Alarm	P+3	dBm	3
26-27	2	TX Power Low Alarm	P-3		
28-29	2	TX Power High Warning	P+2		
30-31	2	TX Power Low Warning	P-2		
32-33	2	RX Power High Alarm	P_0+3	dBm	4
34-35	2	RX Power Low Alarm	P_S-2		
36-37	2	RX Power High Warning	P_0+2		
38-39	2	RX Power Low Warning	P_S		
40-45	16	Reversed			
56-91	36	External Calibration Constants			
92-94	3	Reversed			
95	1	Checksum			5
96-97	2	Real Time Temperature			
98-99	2	Real Time Supply Voltage			
100-101	2	Real Time Tx Bias Current			
102-103	2	Real Time Tx Optical Power			
104-105	2	Real Time Rx Received Power			
106-109	4	Reserved			
110	1	Optional Status/ Control Bits			6
111	1	Reserved			
112-119	8	Optional Set of Alarm and Warning			7

Notes:

1) T_C: Case operating temperature.
2) I_{OP}: Operating current at room temperature. The min. setting current is 0 mA.
3) P: Operating optical power of transmitter at room temperature.
4) P_0: Overload optical power of receiver.
   P_S: Sensitivity optical power of receiver.
5) Byte 95 contains the low order 8bits of sum of bytes 0-94.

6)

State/ Control Bits

Byte	Bit	Name	Description
110	7	Tx Disable State	Digital state of the Tx disable input pin
110	6	Soft Tx Disable	Read/ Write bit that allow software disable of laser
110	5	Reserved	
110	4	Rate Select tate	NA
110	3	Soft Rate Select	NA
110	2	Tx Fault	Digital state of the Tx fault output pin
110	1	LOS	Digital state of the LOS output pin.
110	0	Data_Ready_Bar	NA

7)

Optional Set of Alarm and Warning

Byte	Bit	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
112	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
112	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
112	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
112	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
113	7	Rx Power High Alarm	Set when received power exceeds high alarm level
113	6	Rx Power Low Alarm	Set when received power is below low alarm level
113	5-0	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level
116	6	Temp Low Warning	Set when internal temperature is below low warning level
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level
116	4	Vcc Low Warning	Set when internal supply voltage is below low warning level
116	3	Tx Bias High Warning	Set when Tx Bias current exceeds high warning level
116	2	Tx Bias Low Warning	Set when Tx Bias current is below low warning level
116	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
116	0	Tx Power Low Warning	Set when Tx output power is below low warning level
117	7	Rx Power High Warning	Set when received power exceeds high warning level
117	6	Rx Power Low Warning	Set when received power is below low warning level
117	5-0	Reserved	

Digital Diagnostic Monitor Accuracy

Parameter	Typical Value	Note
Transceiver Temperature	± 3℃	1
Power Supply Voltage	± 3%	2
TX Bias Current	± 10%	
TX Optical Power	± 1.5dB	
RX Optical Power	± 3dB	

Notes:

1) Temperature is measured internal to the transceiver.

2) Voltage is measured internal to the transceiver.

Regulatory Compliance

Test Item	Reference	Qty'	Evaluation
(#1) Electromagnetic Interference EMC	FCC Class B EN 55022 Class B CISPR 22	5	(1) Satisfied with electrical characteristics of product spec. (2) No physical damage
(#2) Immunity： Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 1000-4-3	5	
(#3) Immunity： Electrostatic Discharge to the Duplex SC Receptacle	EN 61000-4-2 IEC 1000-4-2 IEC 801.2	5	
(#4) Electrostatic Discharge to the Electrical Pins	MIL-STD-883C Method 3015.4 EIAJ#1988.3.2B Version 2, Machine model	5	